AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A circuit comprising:

an array of cells operably connected according to a sequence, each of the cells including:

a multiplexer, said multiplexer receiving a plurality of first bit streams, ~~one of said first bit streams conforming to a first format;~~

a space control register coupled to control the multiplexer, and ~~;~~

a latch coupled to receive a signal from the multiplexer; and

a control circuit coupled to control the latch of each of the cells ~~, the control circuit~~ to select one or more bits from a stream of bits output by the multiplexer of each of the cells, wherein

at least one cell in the sequence is coupled to a previous cell in the sequence in order to receive one or more bits output by the previous cell. ~~to thereby generate a second bit stream conforming to a second format.~~

2. (Original) The circuit of claim 1 wherein the multiplexer comprises a plurality of multiplexers.

3. (Original) The circuit of claim 2 wherein the plurality of multiplexers comprise first, second, third, fourth, and fifth multiplexers.

4. (Original) The circuit of claim 3 wherein the first, second, third and fourth multiplexers are 8:1 multiplexers.

5. (Original) The circuit of claim 3 wherein the fifth multiplexer comprises a 6:1 multiplexer coupled to receive an output from the first multiplexer, an output from the second multiplexer, an output from the third multiplexer, an output from the fourth multiplexer, a logical "one", and a logical "zero".

6. (Original) The circuit of claim 1 wherein the space control register programmably stores a value indicating a selected bit from a plurality of bits.

7. (Currently Amended) The circuit of claim 1 wherein the control circuit comprises:

a time control register to store a value indicating a selected bit from a sequence of bits;

a counter to count bits in the sequence of bits from a predetermined bit; and

a comparator coupled to the time control register and to the counter to generate a load signal when a value stored in the time control register and a value provided by the counter are equal, the load signal to cause the latch of a cell in the sequence to load a value output by the multiplexer of that cell.

8. (Currently Amended) The circuit of claim 1 further comprising:

a second multiplexer ~~coupled~~ in the at least one cell configured to receive a signal output by the latch and to receive ~~a~~ the signal output by ~~another circuit~~ the previous cell; and

a second control circuit to control the second multiplexer.

9. (Currently Amended) The circuit of claim 8 further comprising a second latch ~~coupled~~ in the at least one cell configured to receive a signal output by the second multiplexer.

10. (Original) The circuit of claim 1, wherein the multiplexer receives logical values to generate alarm signals.

11. (Currently Amended) A method in a cell, which is implemented in an array of cells operably connected according to a sequence, the method comprising:

receiving multiple first streams of bits at a multiplexer in the implemented cell; ~~, at least one of said bit streams conforming to a first format;~~

selecting one or more bits from one of said received multiple first streams of bits to be latched within the implemented cell based, at least in part, on a space control register value and a time control register value;

receiving at the implemented cell one or more bits output by a previous cell in the sequence; and

outputting a second stream of bits including said selected one or more bits and the one or more bits received from the previous cell. ~~, said second stream of bits conforming to a second format.~~

12. (Original) The method of claim 11 wherein the space control register indicates a selected stream of data from a plurality of streams of data.

13. (Original) The method of claim 12, wherein the space control register is programmable.

14. (Original) The method of claim 11, wherein the time control register indicates one or more bits from a selected stream of data.

15. (Original) The method of claim 14, wherein the time control register is programmable.

16. (New) The circuit of claim 1, wherein the at least one of the cells is configured to:

output the one or more bits from the previous cell during an interval in which no bits are selected by the at least one cell's latch, and

output the one or more selected bits during an interval in which the at least one cell's latch selects the one or more selected bits.

17. (New) The circuit of claim 1, wherein

the stream of bits output by the multiplexer of the at least one cell conforms to a first format, and

the at least one cell outputs the one or more selected bits in such a manner as to output a second bit stream corresponding to a second format.

18. (New) The method of claim 11, wherein the outputting the second stream of bits includes:

outputting the one or more bits received from the previous cell during an interval in which no bits are latched by the implemented cell.

19. (New) The method of claim 18, wherein the outputting the second stream of bits includes:

outputting the one or more selected bits during an interval in which the implemented cell latches the one or more selected bits.

20. (New) The method of claim 11, wherein

the one of said received multiple first streams of bits conforms to a first format, and

the implemented cell outputs the second stream of bits such that the second stream of bits conforms to a second format.